ABSTRACT

A memory controller system is provided including a plurality of memory controller subsystems each coupled between memory and one of a plurality of computer components. Each memory controller subsystem includes at least one queue for managing pages in the memory. In use, each memory controller subsystem is capable of being loaded from the associated computer component independent of the state of the memory. Since high bandwidth and low latency are conflicting requirements in high performance memory systems, the present invention separates references from various computer components into multiple command streams. Each stream thus can hide activate bank preparation commands within its own stream for maximum bandwidth. A page context switch technique may be employed that allows instantaneous switching from one look ahead stream to another to allow low latency and high bandwidth while preserving maximum bank state from the previous stream.